A Lower Conversion Ratio based IBC with Fuzzy PI Control

Vikas K Bhushan, Greeshma Thankam Philip

Abstract— In conventional buck converter, the conversion ratio or the duty cycle is greater than 40% which leads to higher conversion ratio, having discontinuous current and high electromagnetic interference. In order to minimize these above mentioned disadvantages in conventional interleaved converter, a new topology based on artificial intelligence is introduced in this paper. The proposed IBC works in closed loop control with fuzzy accompanied by Proportional-Integral controller which helps to regulate the desired output values at most accurate. The output value is thoroughly verified by the controller unit through a feedback from the output of proposed converter and if there is a change in desired value, the system precisely controls the duty cycle in the converter. The MATLAB software is used to carry out simulations in which the Simulink model were discussed in detail in order to evaluate the overall performance of the converter.

Index Terms— : Duty cycle,Electromagnetic Interference, Fuzzy Logic Controller, Interleaved Buck Converter, Conversion Ratio.

1 Introduction

THE power supply for devices such as battery chargers, solar power regulators, microprocessors and so on, is usually obtained using the buck power conversion which has a lower current ripple. It is achieved usually by increasing the frequency of switching. However, the semiconductor losses increased due to the increase in switching frequency. The conventional buck converter was used widely for dc-dc conversion at step-down level, for non-isolation requirement. The main drawback of the conventional buck converter is the discontinuous input current, which may cause the electromagnetic interference (EMI) in the system. The electromagnetic interference can be reduced if and only if the current flowing through the converter is made continuous which also helps in reducing current stress in the capacitor which is coupled in the input level. As discussed in [1], the converter should operate at higher frequencies for better dynamics and higher power density. But the losses during turn on, turn off etc. that is termed as switching losses increases rapidly with increase in switching frequency. It also deteriorates the efficiency further more. Also it will have a very short duty cycle in cases where output voltage is very low as compared to high input voltage.

In [2], an IBC operating with zero current transition has been discussed. It has also been noted that the diode reverse recovery loss has also been reduced in the topology. A low switch voltage stress in interleaved converter with a novel transformer-less topology is discussed in [3] which consist of two input capacitors which are parallel discharged and series charged. The voltage stress is reduced by the voltage divider circuit present in the converter. As the number of components increases the converter gets complicated and results in increasing the interference which was the main drawback of the circuit. An interleaved buck converter with the aid of a snubber circuit is introduced in [4] consisting a single-capacitor turn-off method. During turn off, the switching loss is reduced and the inductor which is coupled act as two output inductors. But high current stress is affected to all elements due to discontinuous conduction in the circuit which results in high conduction losses and the voltages across all the semiconductor devices are having the input voltage Vin of the converter. As discussed in [5], all switches are turned ON with zero-voltage switching or popularly known as ZVS which consist of an active-clamp circuit with interleaved converter having a high buck conversion ratio. But, the cost increases significantly as the converter requires additional elements such as switches and other semiconductors in order to obtain the above mentioned advantages. As discussed in [6] they introduced zero current transition based interleaved stepdown converter which is designed to reduce diode reverse recovery losses also known as ZCT based interleaved buck converter. The only difference from conventional IBC is that it contains an additional inductor. However, the converter is having high current stress due to the complementary way of current flow in the output path in each module. Also the proposed one is having the main drawbacks of the conventional interleaved structure. As discussed in [7], they introduced two extra phase windings, which extends the duty cycle of the same. Due to the leakage inductance voltage spike were caused and to reduce its effects, an extra clamp circuit has been added to the circuit. Thus, the complexity is increased in the circuit.

In an interleaved converter, the current which is shared between the phases must be balanced. Any imbalance can cause one phase to operate in discontinuous conduction and the other to operate in continuous conduction which can be due to change in duty ratio. According to H. Mao [8], current sharing comparison study is carried out in non-isolated interleaved converters and also in isolated converters. In [9], the analysis of the passive components used in the interleaved structure is discussed. Overrate of paper on the size of the converter results in loss reduction of passive components.

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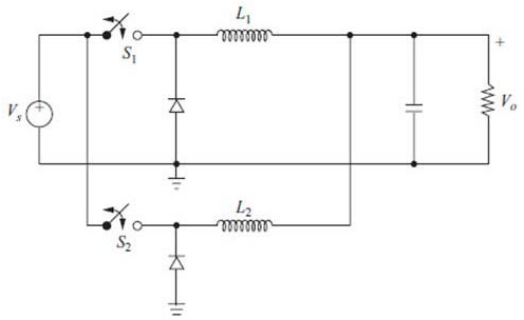

Fig. 1. Conventional IBC

The design of the passive elements and the necessary relation in the phases of interleaved stepdown converter should be given.

Usually the gate signals to the switches of the interleaved converters are provided with pulse width modulation. According to J. A. A. Qahouq, J. Luo and I. Batarsech in [10], the views on hysteretic controller which provides the required pulses for an interleaved converter with N number of phases is explained deliberately. In Fig. 2 control pulse generation circuit is observed which is suggested in [10], for two and four interleaved phases in Fig. 3 respectively.

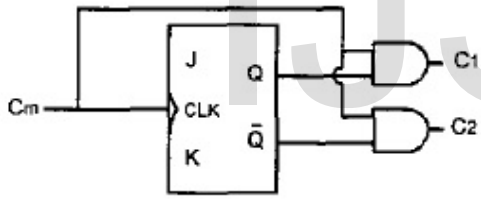

Fig. 2. Pulse generation circuit for two interleaved phases

An interleaved buck converter with ongoing supply current is established into this paper. To decrease the semiconductor voltage stress, the proposed converter fundamentally consists of two input switches. The proposed one is having continuous current at the input side and also has an improved buck conversion ratio as compared to the conventional interleaved buck converter. Also due to the interleaved structure of the proposed converter, the output current ripple is also highly reduced. OCC technique is employed to provide the gate pulses which provide the benefit of faster transient response time.

The paper is arranged in the following order as the circuit configuration is in Section II, the converter operation is in Section III, control strategy employed is described in Section IV. The Section V consist of the simulation along with the results and lastly, the conclusion is given in Section VI.

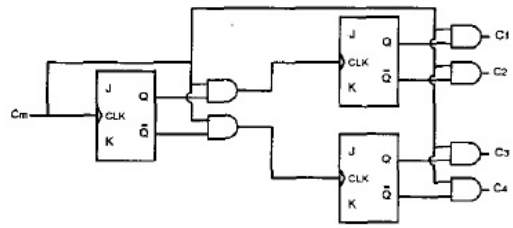

Fig. 3. Pulse generation circuit for four interleaved phases

2 Configuration of Circuit

Fig.4 shows the designed IBC with lower switching losses and current ripple and the topology consists of two freewheeling diodes D1 and D2, two switches Q1 and Q2 which are triggered apart of 180 degrees, two inductors L1 and L2, a coupling capacitor CB and an output capacitor Co. The voltage stress experienced by the switches and diodes are reduced due to the series arrangement of switches.

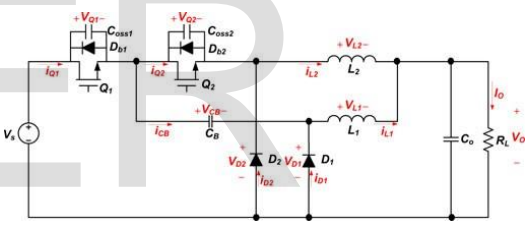

Fig. 4. Proposed IBC (Interleaved Buck Converter)

The conventional IBC has the disadvantage of low on-time during high step-down value and also during high frequency applications. Thus, the IBC operates with lower efficiency when operated at higher switching frequency. The voltage conversion ratio of the conventional interleaved buck converter and buck converter is equal to the duty ratio D. The conventional IBC has voltage stress at the switch side of input whereas the voltage stress experienced by the converter shown in Fig.4 is V in / (2-D) which is less as compared with above mentioned.

3 Converter Operation

Initially, the switches Q1 and Q2 are OFF and both the freewheeling diodes are forward biased. The capacitor has been charged. The converter operation for duty cycle between 0 and 1 has been explained into two parts i.e. operation at D less than 0.5 and operation of D greater than or equal to 0.5.

3.1 Operation for D < 0.5

Mode 1 [t_0 –t_1]: Mode 1 starts when the first semiconductor switch Q_1 is turned ON at t_0. Now the current I_{L1}, flows through Q_1, C_B, and L_1. V_{CB} gets charged and the current of L_2, freewheels through D_2. At this mode, the current through inductor L_1 increases linearly with time and that of L_2 decreases linearly. At Q_2, input voltage will be the terminal voltage and at D_1, the terminal voltage is equal to the difference of V_S and V_{CB}.

Mode 2 [t_1 –t_2]: At t_1 when Q_1 is turned OFF Mode 2 begins. Then, through D_1 and D_2, $i_{L1}(t)$ and $i_{L2}(t)$ freewheels and $V_{L1}(t)$ and $V_{L2}(t)$ becomes -V_O. Hence, current through both inductors decreases linearly. The voltage at the Q_1 terminal is the result of difference between V_S and V_{CB} and voltage across Q_2 becomes the voltage across the coupling capacitor C_B.

Mode 3 [t_2 –t_3]: The third mode of operation starts when diode D_2 is turned OFF and the switch Q_2 is turned ON at t_2 on the same time. Then, inductor current of L_1, which is in series with the semiconductor switch Q_1 that is $i_{L1}(t)$ freewheels through diode D_1 and inductor current at L_2, $i_{L2}(t)$ flows through diode, coupling capacitor, switch, and inductor i.e. through D_1-C_B-Q_2-L_2. Thus V_{CB} is discharged. $V_{L2}(t)$ is the difference between V_{CB} and V_O and is positive. Hence, $i_{L2}(t)$ increases linearly.

Mode 4 [t_3 –t_4]: Mode 4 begins at t_3 when Q_2 is turned OFF and its operation is the same as that of mode 2.

At steady state, under the operating condition of D ≤ 0.5 voltage stress except for Q_2 is determined by V_{CB}. The voltage across the coupling capacitor will be the voltage across switch Q_2 during before turn-on or after turn-off but the maximum value would be the input voltage and due to these results, the discharging of coupling capacitor C_B is reduced to a critical low value and the switching losses thus can be minimized. The conduction losses and reverse recovery characteristics can be improved by using schottky diodes for D_1 and D_2.

3.2 Operation for D > 0.5

Mode 1 [t_0–t_1]: Mode 1 begins when switch Q_1 is turned ON and switch Q_2 is in on-state at t_0 then, the current flows through the switch Q_1, coupling capacitor C_B, and inductor L_1 get charged. Current of inductor L_2 flows through the switches Q_1, Q_2, and through inductor L_2. The inductor voltage is positive.

Mode 2 [t_1 –t_2]: When the switch Q_2 is turned OFF at t_1, Mode 2 begins. Then, current at inductor L_1 flows through the switch Q_1, coupling capacitor C_B, and inductor L_1 and $i_{L2}(t)$ freewheels through diode D_2. The operation is the same as mode 1 in the operation of D ≤ 0.5.

Mode 3 [t_2 –t_3]: The operation is the same with mode 1 and it begins when Q_2 is turned ON at t_2.

Mode 4 [t_3 –t_4]: Mode 4 begins when Q_1 is turned OFF at t_3. Then, through D_1, $i_{L1}(t)$ freewheels and through D_1, C_B, Q_2 and L_2, $i_{L2}(t)$ flows. Thus, V_{CB} is discharged. The operation during this mode is the same with mode 3 in the case of D ≤ 0.5.

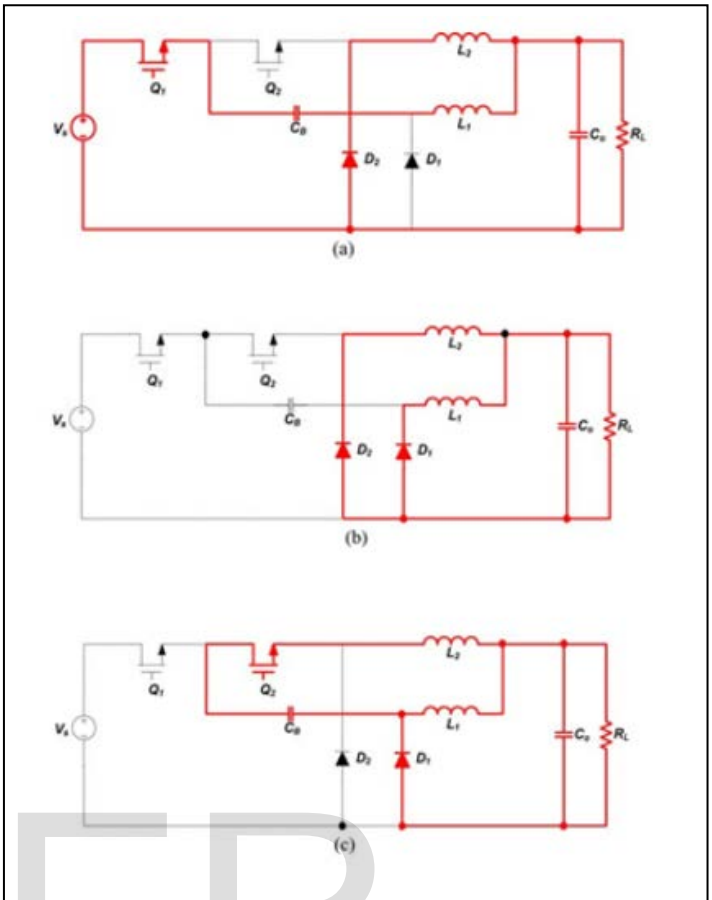

Fig. 5. Operating Circuits when D < 0.5. (a) mode1 (b) mode2 (c)mode3

The proposed interleaved step-down converter operating with duty ratio greater than 0.5 under steady state operating condition is described. Under this, the voltage stress of semiconductor switch Q_1 and diode D_1 is determined by Coupling capacitor voltage, but the voltage stress of semiconductor switch Q_2 and the diode D_2 is achieved by the input voltage. Switches Q_1 and Q_2 experience high current stress in the case of D > 0.5.

4 Control Strategy

Using open-loop control technique is the simplest method to trigger a switch. But the output is independent of load variation, i.e., appropriate adjustments are not able to made by the control system. To overcome the disadvantages of the open-loop control scheme, closed-loop control techniques were introduced The closed-loop control schemes provide adjustments in the duty ratio according to the variations in the line and load. Pulse Width Modulation (PWM) control technique is the commonly used closed-loop control scheme. In PWM control the duty ratio is varied such that the difference between the reference value and the actual value is reduced. When the line or load changes the duty ratio does not sense the error immediately. Thus, the PWM control has a slow response time. Due to the slow response, a transient over-shoot is produced. In order to reach steady-state a large number of cycles are required. In order to obtain load regulation a PI controller is added along with the fuzzy logic.

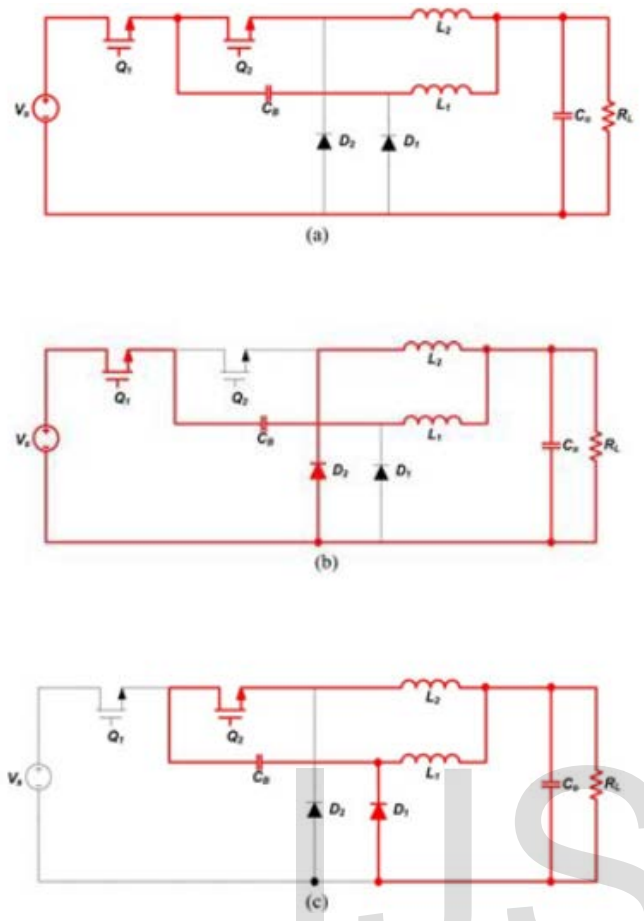

Fig. 6. Operating Circuits when D > 0.5. (a) mode1 (b) mode2 (c) mode3

Since the fuzzification is the sub category of artificial intelligence, it has the advantages such as simple to design and does not require the knowledge of an exact model. According to the basic concept, the fuzzy logic control is having two input variables which are named as Error and Change in Error i.e. E and CE respectively and for every controller there should be an output. Here the output is the duty cycle which is denoted as D. Out of the two output variable in the fuzzy logic controller, by taking the variable E which is the input set as the first one and it is transformed in terms subsets which are represented as NB, NS, ZE, PS and PB which stands for negative big, negative small, zero, positive small and positive big respectively. The detailed graphed membership functions for the input variable E which stands for error in the fuzzy logic subsets are shown in Figure7.

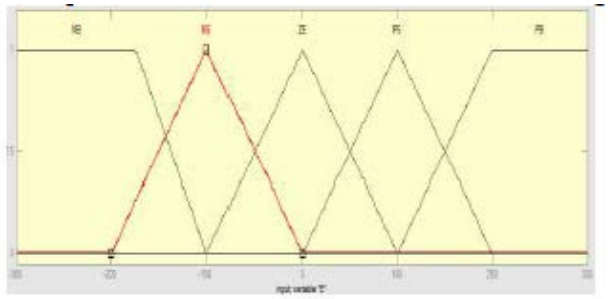

Fig. 7. Input variable E's membership functions.

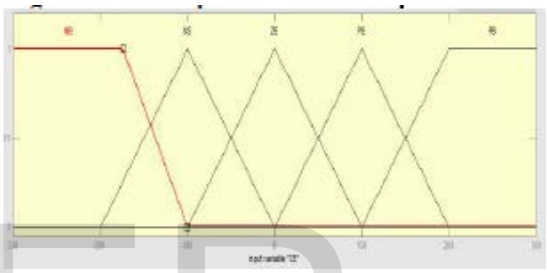

Fig. 8. Input variable CE's membership functions.

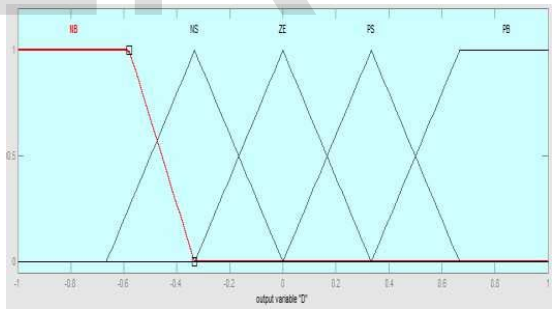

Fig. 9. Input variable D's membership functions

Now the set of the CE is taken as the second input to the fuzzy logic controller which is the change in error and classified into five subsets which are NB, NS, ZE, PS and PB which are negative big, negative small, zero, positive small and positive big respectively. Here the second input variable CE or change in error is also a membership functions for the input side and is shown in figure8. Lastly the justification subset which is used to justify for the output variable which is the duty ratio, D is given in Figure9. The fuzzy logic controller works on a rule base which is created in figure 10 with input variables Error and Change of Error as inputs while D subset as the output. The fuzzy rule matrix table is given below.

CE \ E	NB	NS	ZE	PS	PB
NB	NB	NB	NB	NS	NS
NS	NB	NS	NS	NS	PS
ZE	NB	NS	ZE	PS	PB
PS	NS	PS	PS	PS	PB
PB	PS	PS	PB	PB	PB

Fig. 10. Fuzzy rules

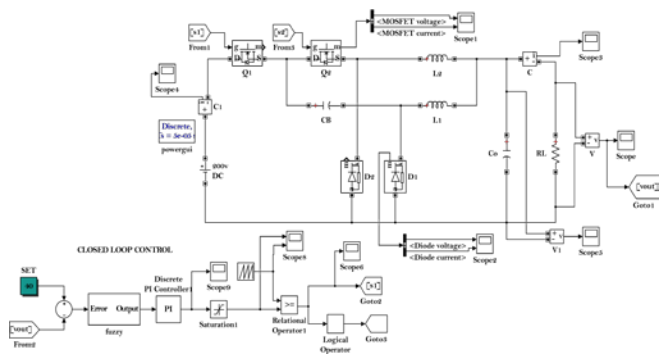

Fig. 11. Simulink Model

5 Simulations

The simulation of the interleaved buck converter with continuous supply current has been carried out for a power level of 240W. The Simulink model using MATLAB software of proposed interleaved buck converter with lower duty cycle is shown in Fig. 10. An input voltage of 200V is applied to the converter and a switching frequency of 100 kHz is chosen and an output of 24V/10A is obtained. The corresponding parameter values used for the simulation of the converter has been listed in Table I.

Here a voltage of 200V is applied at the input and the input current waveform is shown in Fig.12. The output voltage waveform which is termed as VO and the output current, termed as IO waveform can be seen in Fig.13. It can be viewed from the Fig.13 that a constant 24V output has been obtained and also a continuous input current has also been obtained. Also, the output ripple current has been greatly reduced. Fig. 14 shows the inductor current waveforms IL0, IL1 and IL2. Fig. 15 shows the voltage and current stress experienced by the switches and Fig. 16 shows the voltage and current stress experience by the diodes. Since the modes of operation are symmetrical only one switch and diode stress is shown. The voltage stress experienced by the diodes and the switches is approximately equal to 110 V, i.e., the voltage stress present across the semiconductor devices is less than the input voltage.

TABLE 1
Parameter Values

Parameters	Values
Input Voltage	200 V
Output Voltage	24 V
Power Level	240 W
Switching Frequency	100kHz
L_1 and L_2	100μH
L_o	5 μH
C_o	1 μH

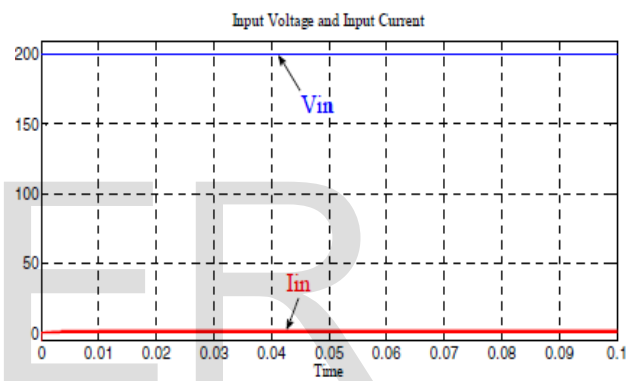

Fig. 12. Input voltage and input current waveform

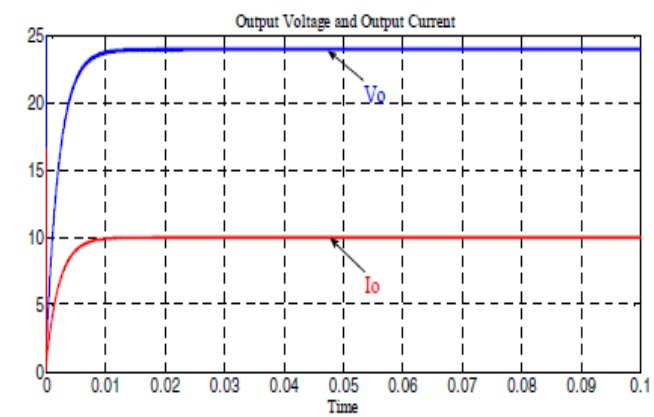

Fig. 13. Output voltage and output current waveform

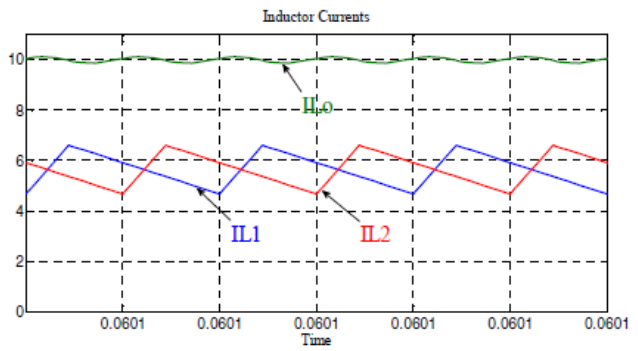

Fig. 14. Inductor current waveform

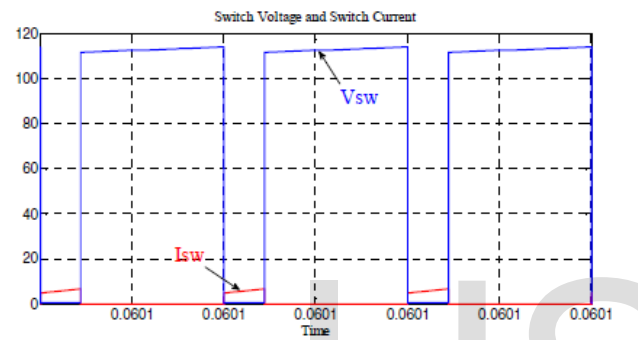

Fig. 15. Switch voltage and switch current waveform

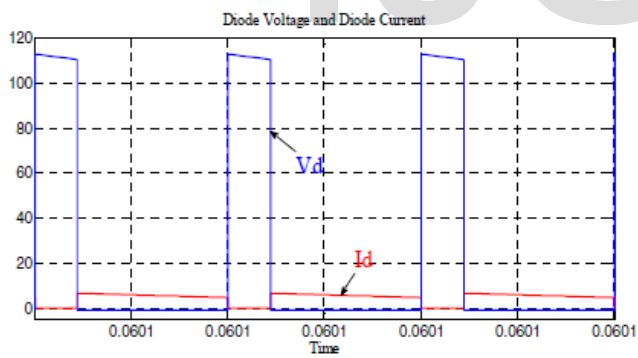

Fig. 16. Diode voltage and diode current waveform

6 Conclusion

In this paper, the main features of the proposed interleaved buck converter have been discussed. Mainly the switching losses are reduced considerably due to the interleaved structure of the proposed converter. Also, the buck conversion ratio of the converter as compared to the conventional IBC, has been improved. The features of the converter also include lower output current ripple. The simulation of the circuit has been carried out using MATLAB software.

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